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EXAMINER	
SPITTLE, MATTHEW D	
ART UNIT	**PAPER NUMBER**
2111	

DATE MAILED: 09/05/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/828,910	NGUYEN ET AL.	
	Examiner	Art Unit	
	Matthew D. Spittle	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 June 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 3-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 3-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1 and 3 – 16 have been examined.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 11, 12 and 16 are rejected under 35 U.S.C. 102(b) as being anticipated by Sytwu (U.S. 5,572,688).

Regarding claim 11, Sytwu describes a method of providing a bus in a computer system comprising:

Routing a first portion of the bus (interpreted as a PCI bus; Figure 3, item 42) to a first segment of a first slot (Figure 3, item 112; Figure 4, item 112);

Routing a second and different portion of the bus (interpreted as an ISA bus; Figure 3, item 60) to a first segment of a second slot (Figure 3, item 114; Figure 4, item 114);

Coupling a second segment of the first slot via at least one trace to a second segment of the second slot (Figure 4, item 116);

Inserting a jumper board into the first slot (Figure 3, item 111; Figure 4, item 111);

Wherein the slots are implemented together on a board other than the jumper board (Figure 4 shows the slots implemented on a backplane (96)).

Wherein the jumper board connects the first and second segments of the first slot, thereby routing the first portion of the bus to the second slot via the at least one trace, while the jumper board does not occupy the second slot (Figure 4 shows the jumper board (111) occupying the first slot).

Regarding claim 12, Sytwu describes wherein the first and second portions of the bus comprise the entire bus (Examiner interprets the bus as a combination of the PCI bus and ISA bus as provided by the bridge (Figure 3, item 52)).

Regarding claim 16, Sytwu describes wherein the connection between slots occurs on a system board (Examiner notes that the connection between the first and second slots occurs both on a system board (Figure 4, item 111) as well as a bridge cable (Figure 4, item 116), and therefore meets this limitation).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1 and 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sytwu (U.S. 5,572,688) in view of Clouser et al. (U.S. 5,884,053).

Regarding claim 1, Sytwu teaches a computer system comprising:

A central processing unit (CPU) (Figure 3, item 22);

A bridge coupled to the CPU for providing a bus (Figure 3, item 52; where the coupling is through the PCI controller (40));

A first slot configured to receive a device, wherein a first portion of the bus is coupled to the first slot (Figure 3, item 112; Figure 4, item 112);

A second slot configured to receive a device, wherein a second and different portion of the bus is coupled to the second slot (Figure 3, item 114; Figure 4, item 114);

At least one trace coupled to the first and second slots (Figure 4, item 116);

Wherein the computer system is configured so that inserting a jumper board (Figure 3, item 111; Figure 4, item 111) in the first slot couples the first portion of the bus to the second slot via the at least one trace, while the jumper board does not occupy the second slot (Figure 3 shows the jumper board (111) occupying only the first slot (112), while the trace (bridge cable) occupies the second slot));

Wherein the slots are implemented together on a board other than the jumper board (Figure 4 shows the slots implemented on a backplane (96)).

Sytwu fails to teach the bus having lanes, where a lane is interpreted by Examiner to be a differential pair of data lines, consistent with Applicant's disclosure.

Clouser et al. teach using differential data lines with a PCI bus for the purpose of reducing noise, using less energy, and providing for faster transfer rates (column 2, lines 22 – 27; column 4, lines 41 – 51).

Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by applicant to incorporate differential signaling as taught by Clouser et al. in the system of Sytwu for the purpose of improving bus performance.

Regarding claim 3, Sytwu teaches the additional limitation wherein each slot is capable of providing all signals pertaining to the bus (Examiner interprets the bus as a combination of the PCI bus and ISA bus as provided by the bridge (Figure 3, item 52),

therefore, since the first slot is a PCI slot and the second slot is an ISA slot (column 4, lines 30 – 35), they inherently are able to provide all signals pertaining to their respective buses through the jumper board (Figure 3, item 111; Figure 4, item 111)).

95 * * *

Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sytwu (U.S. 5,572,688) in view of Clouser et al. (U.S. 5,884,053) and Potter et al. (U.S. 6,533,587).

100 Regarding claim 4, Sytwu teaches a computer system comprising:

A central processing unit (CPU) (Figure 3, item 22);

A bridge coupled to the CPU for providing a bus (Figure 3, item 52; where the coupling is through the PCI controller (40));

A first slot configured to receive a device, wherein a first portion of the bus is

105 coupled to the first slot (Figure 3, item 112; Figure 4, item 112);

A second slot configured to receive a device, wherein a second and different portion of the bus is coupled to the second slot (Figure 3, item 114; Figure 4, item 114);

At least one trace coupled to the first and second slots (Figure 4, item 116);

A jumper board (Figure 3, item 111; Figure 4, item 111);

110 Wherein the computer system is configured so that inserting the jumper board in the first slot couples the first set portion of the bus to the second slot (Figure 4 shows

the riser board couples the first bus (PCI) to the second slot (ISA slot) via the bridge cable (116)).

Sytwu fails to teach the bus having lanes, where a lane is interpreted by Examiner to be a differential pair of data lines, consistent with Applicant's disclosure.

Clouser et al. teach using differential data lines with a PCI bus for the purpose of reducing noise, using less energy, and providing for faster transfer rates (column 2, lines 22 – 27; column 4, lines 41 – 51).

Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by applicant to incorporate differential signaling as taught by Clouser et al. in the system of Sytwu for the purpose of improving bus performance.

Sytwu and Clouser et al. fail to teach wherein the slots are implemented on a riser board.

Potter et al. teach using a riser board for the purpose of improving reducing the length of the interconnecting bus between components on the riser board, allowing for better air flow around the expansion devices on the riser card, and consuming less space in mounting the expansion devices on the riser card (column 2, lines 51 – 55; column 5, lines 10 – 39).

Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by applicant to incorporate a riser board as taught by Potter et al. into the computer system of Sytwu and Clouser et al. for the purpose of providing less propagation delay (due to reduced length of bus interconnects), and thus better performance, as well as extending the life of the expansion devices on the riser card

(due to better cooling), and allowing the enclosure to be made smaller (due to the riser card mounting means taking up less space).

* * *

Claims 5 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sytwu (U.S. 5,572,688) in view of Clouser et al. (U.S. 5,884,053) and Potter et al. (U.S. 6,533,587) and Intel Corporation.

Regarding claims 5 and 6, Sytwu, Clouser et al., and Potter et al. fail to teach lane polarity inversion techniques on a printed circuit board that includes first and second slots, and also fails to teach lane reversal techniques on a printed circuit board that includes first and second slots.

Intel Corporation teaches using lane polarity inversion and lane reversal for the purposes of eliminating "bowties" on a printed circuit board (page 7, section 1.2.2 – page 9).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to incorporate lane polarity inversion and lane reversal techniques on a printed circuit board that includes the first and second slots for the purpose of reducing and/or eliminating "bowties." This would have been obvious in order to reduce the cost of the PCB by reducing the size, complexity, or number of necessary layers.

* * *

Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sytwu (U.S. 5,572,688) in view of Clouser et al. (U.S. 5,884,053) and Shipe (U.S. 6,780,018).

Regarding claim 7, Sytwu teaches a computer system comprising:

A central processing unit (CPU) (Figure 3, item 22);

A bridge coupled to the CPU for providing a bus (Figure 3, item 52; where the coupling is through the PCI controller (40));

A first slot configured to receive a device, wherein a first portion of the bus is coupled to the first slot (Figure 3, item 112; Figure 4, item 112);

A second slot configured to receive a device, wherein a second and different portion of the bus is coupled to the second slot (Figure 3, item 114; Figure 4, item 114);

At least one trace coupled to the first and second slots (Figure 4, item 116);

Wherein the computer system is configured so that inserting a jumper board (Figure 3, item 111; Figure 4, item 111) in the first slot couples the first portion of the bus to the second slot (Figure 4 shows the riser board couples the first bus (PCI) to the second slot (ISA slot) via the bridge cable (116)).

Wherein the slots are implemented together on a board other than the jumper board (Figure 4 shows the slots implemented on a backplane (96)).

Sytwu fails to teach the bus having lanes, where a lane is interpreted by Examiner to be a differential pair of data lines, consistent with Applicant's disclosure.

Clouser et al. teach using differential data lines with a PCI bus for the purpose of reducing noise, using less energy, and providing for faster transfer rates (column 2, lines 22 – 27; column 4, lines 41 – 51).

Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by applicant to incorporate differential signaling as taught by Clouser et al. in the system of Sytwu for the purpose of improving bus performance.

Sytwu and Clouser et al. fail to teach wherein the first and second sets of lanes of the bus each form a serial bus.

Shipe teaches that PCI Express is a serial bus that offers low-cost, scalable performance and achieves a high performance connection between two electronic devices such as a motherboard and a card (column 1, lines 23 – 43).

Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by applicant to incorporate the serial bus as taught by Shipe into the computer system of Sytwu and Clouser et al. for the purpose of improving computer system performance.

* * *

Claims 8 – 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sytwu (U.S. 5,572,688) in view of Clouser et al. (U.S. 5,884,053), Shipe (U.S. 6,780,018) Gehrke et al. (U.S. 6,310,992).

Regarding claim 8, Sytwu, Clouser et al., and Shipe fail to teach wherein the serial bus comprises an optical bus.

Gehrke et al. teach using a serial bus that comprises an optical bus (column 3, lines 47 – 56) for the purpose of reducing electromagnetic interference from radiating to other devices, thereby increasing the reliability of the system (column 5, line 65 – column 6, line 12).

Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by applicant to use an optical bus as taught by Gehrke et al. in the system of Locker et al. and Shipe to improve the reliability of the system by reducing electromagnetic interference between interconnected modular electrical devices (such as expansion cards).

Regarding claim 9, Shipe teaches the additional limitation wherein the serial bus is a PCI-Express bus (column 1, lines 27 – 34).

Regarding claim 10, Sytwu teaches the additional limitation wherein the slots do not provide connections for all signals pertaining to the bus without the jumper board. Examiner interprets the bus as a combination of the PCI bus and ISA bus as provided by the bridge (Figure 3, item 52), therefore, since the first slot is a PCI slot and the second slot is an ISA slot (column 4, lines 30 – 35), they inherently are able to provide all signals pertaining to their respective buses through the jumper board (Figure 3, item 111; Figure 4, item 111)).

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* * *

Claims 13 – 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sytwu (U.S. 5,572,688) in view of PCI Express and Clouser et al. (U.S. 5,884,053).

225 Regarding claim 13, Sytwu fails to teach selecting the first and second slots from among several available slot configurations to correspond to a maximum number of physical lines of the bus.

PCI Express teaches selecting a slot, from among several available slot configurations, to correspond to a maximum number of physical lines of a bus for the

230 purpose of providing a flexible configuration matched to a particular I/O device's bandwidth and application objectives (section 4.2.4.7.1, pages 166 – 167).

Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by applicant to apply the teachings of PCI Express to the bus of Locker et al. for the purpose of providing a flexible configuration matched to a particular I/O

235 device's bandwidth and application objectives. This would have been obvious in order to accommodate future device requirements, thereby extending the life cycle of the bus.

Sytwu fails to teach the bus having lanes, where a lane is interpreted by Examiner to be a differential pair of data lines, consistent with Applicant's disclosure.

Clouser et al. teach using differential data lines with a PCI bus for the purpose of

240 reducing noise, using less energy, and providing for faster transfer rates (column 2, lines 22 – 27; column 4, lines 41 – 51).

Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by applicant to incorporate differential signaling as taught by Clouser et al. in the system of Sytwu for the purpose of improving bus performance.

Regarding claim 14, PCI Express teaches the additional limitation of adjusting a slot such that it can physically accommodate more than just a portion of the bus for the purpose of providing a flexible configuration matched to a particular I/O device's bandwidth and application objectives (section 4.2.4.7.1, pages 166 – 167).

Regarding claim 15, Sytwu teaches the additional limitation wherein the first and second slots are capable of providing all signals that pertain to the entire bus (Examiner interprets the bus as a combination of the PCI bus and ISA bus as provided by the bridge (Figure 3, item 52)).

Response to Arguments

Applicant's arguments with respect to claims 1 and 3 - 16 have been considered but are moot in view of the new ground(s) of rejection.

260 ***Conclusion***

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

265 A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any 270 extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew D. Spittle whose telephone number is (571) 275 272-2467. The examiner can normally be reached on Monday - Friday, 8 - 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on 571-272-3632. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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